UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,293	11/20/2003	Robert James Blainey	CA920030013US1	1209

46073 7590 07/18/2008

IBM CORPORATION (VE)
C/O VOLEL EMILE
P. O. BOX 162485
AUSTIN, TX 78716

EXAMINER	
ZHE, MENG YAO	
ART UNIT	PAPER NUMBER
2195	

MAIL DATE	DELIVERY MODE
07/18/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/718,293	BLAINEY ET AL.	
	Examiner	Art Unit	
	MENGYAO ZHE	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/24/3008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10,11,14-19 and 22-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8, 10-11, 14-19, 22-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8, 10-11, 14-19, 22-31 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-8, 10-11, 14-19, 22-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishihata et al., Patent No. 5,278,975 (hereafter Ishihata) in view of Matsumoto, Patent No. 5,448,732 (hereafter Matsumoto).

4. Ishihata was cited in the previous office action.

5. As per claims 1, 14, 24, 25, 26, 28, 30, Ishihata teaches a method of synchronizing N concurrently running processes in a data processing system at a first phase before allowing the N processes to proceed to a second phase, N>=2, comprising:

(a) providing a first array of N elements initialized each to a first state, wherein each ith element of said first array is associated with an ith concurrently running process which will update the ith element of the first array to a second state in response to completing the first phase, where 1<=I<=N (Column 4, lines 50-58: the synchronization

request register for each PE corresponds to an element of the array. The register is updated by the PE individually when it has decided to request for synchronization.);

(b) providing a second array of N elements initialized each to a hold state, wherein each ith element of said second array is associated with the ith concurrently running process associated with the ith element of the first array and is used to hold the ith associated concurrently running process at the first phase and is enabled to switch, in response to receiving a release signal, to a release state to release the ith associated concurrently running process to proceed to the second phase (Column 4, lines 63-66; Column 10, lines 39-49: the status detecting register for each PE corresponds to each element of the second array; upon notification from the PEs that all is normal and synchronization detecting register has detected that all synchronization request registers, which corresponds to the first array, are all logics of 1s, the status detection register, which corresponds to the second array changes to a different state, which is the release state.);

(c) ascertaining when the N elements of the first array are updated to the second state to issue the release signal to allow the N processes to proceed to the second phase (Column 4, lines 63-66; Column 9, 58-Column 10, lines 12; The status detection register, which is the second array, turns into a release state, when the synchronization request register, which is the first array, sends out a signal that all array elements are 1s.).

Ishihata discloses hardware connections and setups that allows the steps above to be performed. Ishihata does not specifically teach using a designated process that is able to issue a release instruction such that the release instruction is release when the designated process determines when N elements of the first array are updated to the second state.

However, Matsumoto teaches using a designated process configured to ascertain when the N processes are all synchronized together to terminate the synchronization waiting state and proceed to the second phase by issuing a release instruction (Column 7, lines 35-48; Fig 8, s5, s11, s12, s9: whichever instruction that terminates the synchronization waiting state corresponds to the release instruction.) for the purpose of synchronization among multiple threads.

It would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to modify the teachings of Ishihata with using a designated process configured to ascertain when the N processes are updated to be synchronized to terminate the waiting state and proceed to the second phase by issuing a release instruction, as taught by Matsumoto, because it allows for synchronization among multiple threads.

6. As per claims 2, 29, 31, Ishihata teaches (d) for each process of said at least two concurrently running processes, configuring said each process such that, upon completion of said phase and upon updating of its associated ith element of said first

array, said each process then waits at its associated element of said second array for said release state (Column 10, lines 20-25).

7. As per claim 6, Ishihata teaches wherein after the N elements of said first array are updated to the second state, and prior to issuance of the release signal, the N elements of said first array are reinitialized to the first state (Column 10, lines 40-48).

8. As per claim 8, Ishihata teaches the designated process is not one of the N concurrently running processes (Column 10, lines 49-54).

9. As per claims 10, 18, Ishihata teaches wherein each ith element of said first array and said second array comprises a state machine (Column 4, lines 56-58; Fig 15).

10. As per claims 11, 19, Ishihata teaches wherein said state machine is one of a counter, a gate, a flag and a sensor (Fig 15).

11. As per claim 23, Ishihata teaches wherein said N concurrently running processes execute on multiple processors distributed across multiple computers connect across a network (Column 1, lines 7-15).

12. As per claim 3, 4, 15, 16, Ishihata does not specifically teach wherein each element of said first array has a byte size corresponding to the size of a cache line used in said data processing system. However, it would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to allocate any size for the array as he wishes, including the size of a cache line, so that all data in the array may also fit in the cache line for quicker access.

13. As per claims 5, 17, Ishihata does not specifically teach providing each element of said second array locally in relation to its respective, associated process. However, it would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to have all the element stored locally to its associated process for easier management and access.

As per claims 7 and 27, Ishihata does not specifically teach wherein said designated process is one of said concurrent processes. However, it would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to let one of the concurrently processes be the designated process since it would be more efficient and less resource used if one of the concurrent process can also be used as a control process for the issuing of release instructions instead of using a complete separate process solely dedicated to that purpose.

14. As per claim 22, Ishihata does not specifically teach wherein said at least two concurrently running processes execute on multiple processors embodied within a single computer. However, it would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to have multiple processes executing on multiple processors within a single computer since multi-core processors are available at the time of the invention.

Response to Arguments

15. Applicant's arguments with respect to claims 1-8, 10-11, 14-19, 22-31 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MENGYAO ZHE whose telephone number is (571)272-6946. The examiner can normally be reached on Monday Through Friday, 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195